PROTES
Towards a UML profile for Real-Time Embedded Systems
THALES, INRIA, CEA
Presented by Y. SOREL, Inria
Project coordinator: L. RIOUX, Thales
PROTES: Organisation

- **Partners:**
  - THALES Research and Technology
  - THALES Aerospace
  - THALES Land & Joint
  - THALES Naval / Underwater Systems
  - CEA/LIST (LSP laboratory)
  - INRIA (Aoste, DaRT, Espresso teams)

- **Project timescale:**
  - Started: 15 October 2003
  - Ends: September 2006
  - Duration: 36 months
Motivations

RT Embedded systems are complex because:

- **Pluridiciplinary**: software, hardware, system engineering, control theory & signal processing, physical sensors/actuators,…
- **Heterogeneous**: HW/SW execution platforms, component reuse, reconfigurable hardware, …
- **Stringent requirements**: hard real-time, limited resources, performance/power/cost constraints

Strong tradition of graphical notations and early models (at least more than in traditional computer science), but:

- Used mostly for documentation or prototype simulation
- Approximate semantics (informal)
- Good for tuning specs, less for direct seamless implementation
Industrial domain

- **Typical applications**
  - Cars, planes, satellites
  - Mobile and Wireless telecommunications
  - Signal processing (radar, sonar…)
  - SoC design (Application Specific Processors, …)

- **Modeling should address:**
  - **Reactive systems** *(control modes, communications)*
  - **Control/Command**, supervision *(sensors, actuators)*
  - **Intensive data-flow computation** *(multimedia signal processing)*
  - HW/SW codesign
  - …
Our approach

- **Model-based design**
  - Should use natural, appealing models, and with sound mathematical semantics (*MoCs: models of computation*)

- **Platform-based design**
  - Independent modeling of **functional application** and **execution platform**
  - Subsequent **allocation** of functions to resources, under RT constraints

- **Design/Architecture exploration**
  - **Variations** are possible *both* on application and architecture models
Industrial needs and relevance

- Many existing or emerging design tools and techniques, but scattered and not integrated in a unified framework
  - Ex. Mathlab/Simulink or Scilab/Scicos, Statemate, Ptolemy, Esterel/Scade, ACCORD-UML, AAA-SynDEx, Array-OL, …

- Models should provide support for
  - **Analysis**: schedulability, functional correctness…
  - **Synthesis**: partitioning, scheduling, glue code production

- General trend in UML to head this way
  - UML2.0 activity diagrams, SPT, QoS, SysML
  - *UML4SoC and AADL attempts*

Hence the idea of proposing a dedicated profile for RTE modeling!
Protes Objectives

- **To promote a dedicated UML profile at OMG**
  - To specify real-time and embedded systems in UML, with adequate and sound meaning, using modeling features familiar to engineers
  - To permit the correctness and schedulability analysis of such systems
  - To permit smooth and seamless implementation of the functional algorithmic models onto the HW/SW platform execution models

- **To develop this profile in a UML tool**
  - Fit for integration with the MDE approach used at THALES
  - Providing modeling constructs matching the methodologies and formalisms developed at INRIA and CEA.
General technical Requirements

- **What we want**
  - System-level co-modeling, HW/SW
  - Simulation at different abstraction levels
  - Formal verification and automatic test generation
  - Code generation and hardware synthesis
  - Model-based optimization
  - Heterogeneous target platforms, flexibility

- **What we need**
  - Formal semantics, mathematical model properties
  - Synchronous, GALS, untimed and scheduled models
  - Consistency between modeling views, and traceability links
  - UML-support for models
  - Model Driven Engineering
  - User guidance and methodological elements
RFP Requirements

- **TCR (Time and Concurrent Resources) subprofile**
  - logical asynchronous or synchronous, physical discrete or dense
  - Abstract resources (hardware active/passive components, media, OS schedulers, processor models ?)

- **RTEM (Real-Time Embedded Modeling) subprofile**
  - Application behavior/structural modeling, mixing data-flow and control-flow models
    - Hierarchical FSMs, data-flow block-diagrams, loop iterators
  - Architectural platform behavior/structural modeling, with mixed hardware/software components
  - Allocation modeling for mapping of application onto architecture
  - Non functional stereotype attributes for further analysis/synthesis/optim

- **RTEA (Real-Time Embedded Analysis) subprofile**
  - Largely follow-up of SPT effort
  - Schedulability analysis models
PROTES: Profil UML pour les Systèmes Temps-Réel et Embarqués

Application side

Comm & Control

(Synchronous)

state diagrams

«Meet-in-the-middle»

Data Computation

Activity

(block) diagrams

Allocations

(operations to resources)

Formal models

Structure/deployement diagrams

HW/SW platform model

Architectural side

Model-Based Design

System-Level Design

Platform-Based Design
Current achievements

- Leading actors in the OMG MARTE RFP issued
  
  Now voted and approved!

- Next, gathering a consortium for a joint answer: proMARTE
  
  - Most UML tool vendors
  - Most partners from the former SPT profile (Schedulability, Performance & Time)
  - Some contacts with the UML4SoC and AADL-UML proponents

Initial submission November 2005 (current main concern)
Today: 11 Letters of Intent (LOI)!

for the record, SysML has 9…

- ARTISAN Software Tools
- Alcatel
- I-Logix
- IBM
- Lockheed Martin
- Mentor Graphics Corporation
- Pathfinder Solutions
- Rockwell Collins
- Softeam
- THALES
- 88solutions
Next in PROTES

**In PROTES**

- Start the development of a prototype tool for testing new concepts introduced in the standard.
- Further, developing an pre-industrial prototype UML profile.

**In ProMARTE:**

- Shape up the response document (initial, then updated)
- Keep a balance between our main concerns (RTEM) and the SPT/RTEA schedulability community
- Bridge up gap with UML4SoC and AADL proposals (which address UML-isation at superficial level, but might insist on going solo).
Typical PROTES resources per year on MARTE RFP

- **INRIA:**
  - Permanent staff and academic PhD students
  - 1 junior engineer at INRIA
  - 1 half-time senior engineer at INRIA

- **CEA:**
  - 1 senior engineer at CEA

- **THALES**
  - Participation of THALES R&T, THALES L&J, THALES AE, THALES Computer
    - Coordination and requirements

Active participation of 1-3 Protes members to each OMG TC meeting
- 5 meetings per year

→ OMG participation did double resources on MARTE without loss of direction
Wrap-up: expected results

- **Forthcoming UML profile should:**
  - Use graphical models familiar to designers
  - Possess formal mathematical semantics
  - Provide a unified framework to connect with state-of-the-art powerful analysis and synthesis techniques, as developed in our teams and elsewhere

- **Main benefits:**
  - Schedulability and correctness analysis
  - Seamless code production from high-level description models
  - Flexibility of implementation of functional applications onto architectural SW/HW platforms